AN10857

Application and soldering information for PCF2127A and PCF2129A TCXO RTCs

Rev. 01 — 11 December 2009 | Application note

Document information

Info	Content
Keywords	PCF2127A, PCF2129A, soldering, application, timekeeping, timestamp
Abstract	This application note gives additional information about soldering and application configuration of the PCF2127A and PCF2129A TCXO RTCs

founded by Philips

Revision history

Rev	Date	Description
01	20091211	new application note, first revision

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1. Introduction

This application note provides some additional information on the PCF2127A and PCF2129A. In the following PCF212xA is used for information concerning both types, PCF2127A and PCF2129A.

The accuracy of time given by an RTC[1] is mostly depending on the accuracy of the crystal used. For example a tuning fork crystal resonates at room temperature at its nominal frequency but will slow down when the temperature deviates (see graph no. 2 in Figure 2).

The PCF212xA is a CMOS Real Time Clock (RTC) and calendar IC with an integrated Temperature Compensated crystal (Xtal) Oscillator (TCXO) based on an integrated 32.768 kHz tuning fork quartz crystal optimized for very high accuracy and very low power consumption. It compensates automatically for temperature dependent frequency deviations (see graph no. 1 in Figure 2).

For further information, refer to the appropriate data sheets (Ref. 5 "PCF2127A" and Ref. 6 "PCF2129A").

2. Feature comparison between PCF2127A and PCF2129A

Table 1. Feature comparison list

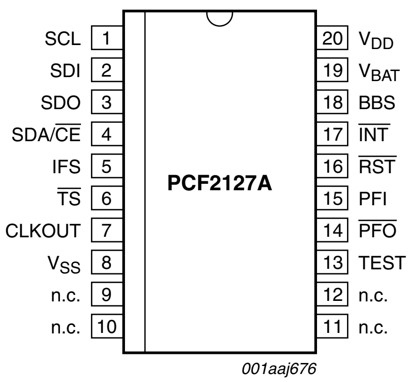
Feature	PCF2127A	PCF2129A
Accuracy (typical)	±3 ppm from –15 °C to +60 °C	±3 ppm from –15 °C to +60 °C
Interface	I^2C- and SPI-bus	I^2C- and SPI-bus
RAM	512 bytes	-
Package	SO20	SO20
Supply voltage range (V_{DD})	1.8 V to 4.2 V	1.8 V to 4.2 V
Battery supply voltage range (V_{BAT})	1.8 V to 4.2 V	1.8 V to 4.2 V
Battery switch over function	yes	yes
Battery low detection function	yes	yes
Extra power fail detection function	yes	no
Battery back end output voltage pin	yes	yes
Reset output pin	yes	no
Countdown timer and watchdog function	yes	watchdog only
Timestamp function	yes	yes

1. The definition of the abbreviations and acronyms used in this document can be found in Section 11.

3. Pinning and register overview

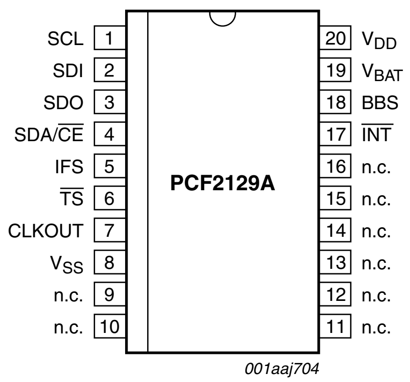
3.1 Pinning diagrams of PCF212xA

Figure 1 shows the pining layout of the PCF212xA. For more detailed information on pinning and pin description see the data sheets Ref. 5 "PCF2127A" and Ref. 6 "PCF2129A".



Top view. For more package and pin related information see Ref. 5 "PCF2127A".

a. Pin configuration of PCF2127A (SO20)



Top view. For more package and pin related information see Ref. 6 "PCF2129A".

b. Pin configuration of PCF2129A (SO20)

Fig 1. Pinning diagrams of PCF212xA

3.2 Register overview

PCF2127A contains 30, PCF2129A 28 8-bit registers (see extract of registers in Table 2 and Table 3).

Table 2. Extract of the PCF2127A registers

Bit positions labeled as - are not implemented and will return a 0 when read; don't care. Bit T must always be written with logic 0. For further information see data sheet Ref. 5 "PCF2127A".

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	EXT_ TEST	T	STOP	TSF1	POR_ OVRD	12_24	MI	SI
01h	Control_2	MSF	WDTF	TSF2	AF	CDTF	TSIE	AIE	CDTIE
02h	Control_3	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE
:	:	:	:	:	:	:	:	:	:
0Fh	CLKOUT_ctl	TCR[1:0]		-	-	-	COF[2:0]		
:	:	:	:	:	:	:	:	:	:
12h	Timestp_ctl	TSM	TSOFF	-	1_O_16_TIMESTP[4:0]				
:	:	:	:	:	:	:	:	:	:
19h	Aging_offset	-	-	-	-	AO[3:0]			

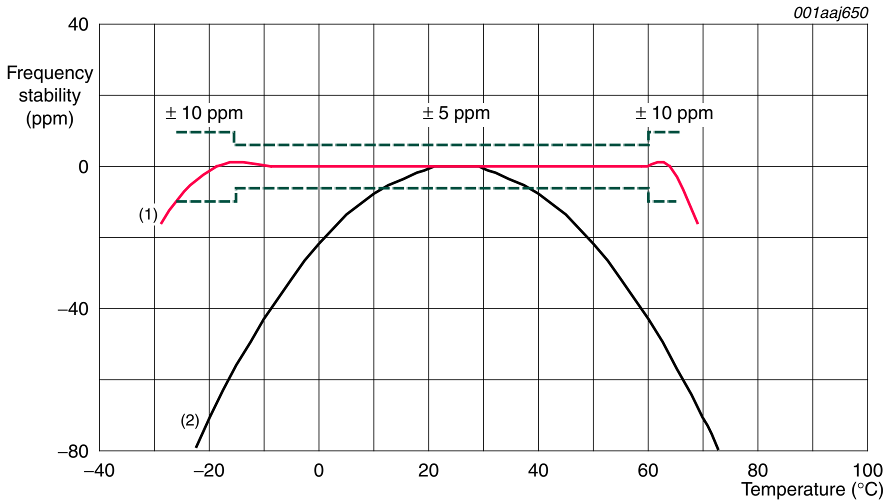
Table 3. Extract of the PCF2129A registers

Bit positions labeled as - are not implemented and will return a 0 when read; don't care. Bits labeled as T must always be written with logic 0. For further information see data sheet Ref. 6 "PCF2129A".

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	EXT_ TEST	T	STOP	TSF1	POR_ OVRD	12_24	MI	SI
01h	Control_2	MSF	WDTF	TSF2	AF	T	TSIE	AIE	T
02h	Control_3	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE
:	:	:	:	:	:	:	:	:	:
0Fh	CLKOUT_ctl	TCR[1:0]		-	-	-	COF[2:0]		
:	:	:	:	:	:	:	:	:	:
12h	Timestp_ctl	TSM	TSOFF	-	1_O_16_TIMESTP[4:0]				
:	:	:	:	:	:	:	:	:	:
19h	Aging_offset	-	-	-	-	AO[3:0]			

4. Frequency stability and time accuracy

Figure 2 shows the frequency stability of PCF212xA with respect to the temperature.



V_{DD} or V_{BAT} = 3.3 V.

(1) Temperature compensated frequency.

(2) Uncompensated typical tuning-fork crystal.

Fig 2. Characteristic of frequency with respect to temperature

Remark:

- For V_{DD} or V_{BAT} other than 3.3 V, a frequency drift of ±1 ppm/V has to be expected.
- The switching from the main power supply V_{DD} to the backup battery V_{BAT} may cause that - depending on the voltage difference - the internal clock stops just after the transition and then recovers again. A voltage transition of 0.3 V from V_{DD} and V_{BAT} or vice versa may typically cause a loss of 10 ms. One incident per 24 h would therefore lead to a deviation of −0.1 ppm.
- For information about frequency correction, see Section 6.4.

5. Frequency measurement

The frequency stability can be evaluated by measuring the frequency of the square wave signal available at the output pin CLKOUT.

The frequency signal at pin CLKOUT is controlled by the COF[2:0] control bits in register CLKOUT_ctl (0Fh) according to Table 4.

Table 4. CLKOUT frequency selection

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]
000	32768	60 : 40 to 40 : 60
001	16384	50 : 50
010	8192	50 : 50
011	4096	50 : 50
100	2048	50 : 50
101	1024	50 : 50
110	1	50 : 50
111	CLKOUT = high-Z	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

The selection of f_{CLKOUT} = 32.768 kHz (COF[2:0] = 000, default value) leads to inaccurate measurements. It is therefore recommended to select a frequency other than the default value of 32.768 kHz for accurate frequency measurements. The most accurate frequency measurement occurs when 1 Hz is selected.

Furthermore, for accurate evaluation of the frequency stability over temperature, it is important that the frequency measurement is executed when the temperature is stable and the PCF212xA performs the temperature measurement. The PCF212xA measures the temperature immediately after power-on and then periodically with a period set by the temperature conversion rate bits TCR[1:0] in register CLKOUT_ctl (0Fh):

Table 5. Temperature measurement period

TCR[1:0]	Temperature measurement period
00 [1]	4 min
01	2 min
10	1 min
11	30 seconds

[1] Default value.

Once the temperature is set and is stable, it is necessary to wait until the PCF212xA has performed the temperature measurement, then the frequency can be measured at the CLKOUT pin. To perform quicker measurements it is recommended to select the temperature measurement period of 30 seconds (TCR[1:0] = 11).

In summary, for an accurate evaluation of the frequency stability the following operating flow is recommended:

- Power-on with V_{DD} = 3.3 V
- Wait until the 32.768 kHz signal is available at the CLKOUT pin

- Program a COF[2:0] value other than the default, for example COF[2:0] = 110, which corresponds to f_{CLKOUT} = 1 Hz
- Program TCR[1:0] = 11, which corresponds to a temperature measurement period equal to 30 seconds
- Set the target temperature
- Wait until temperature is stable
- Wait until the temperature measurement is executed (~30 seconds after the temperature is stable)
- Measure the frequency at the CLKOUT pin.

6. Reflow soldering

6.1 Introduction to reflow soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs) to form electrical circuits. The soldered joint provides both, the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one Printed Circuit Board (PCB); however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

The PCF212xA is intended for use in a reflow soldering process.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile (see Figure 3); this profile includes preheat (T_s), reflow (in which the board is heated to the peak temperature (T_p)) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged.

For further information on reflow soldering IC, refer to Ref. 1 “AN10365”.

6.2 Reflow soldering of PCF212xA

The PCF212xA is intended for use in a lead-free reflow soldering process, classified in accordance with the Ref. 3 “IPC/JEDEC J-STD-020”.

Figure 3 shows the reflow soldering temperature profile according Ref. 3 “IPC/JEDEC J-STD-020” used for the qualification of the PCF212xA.

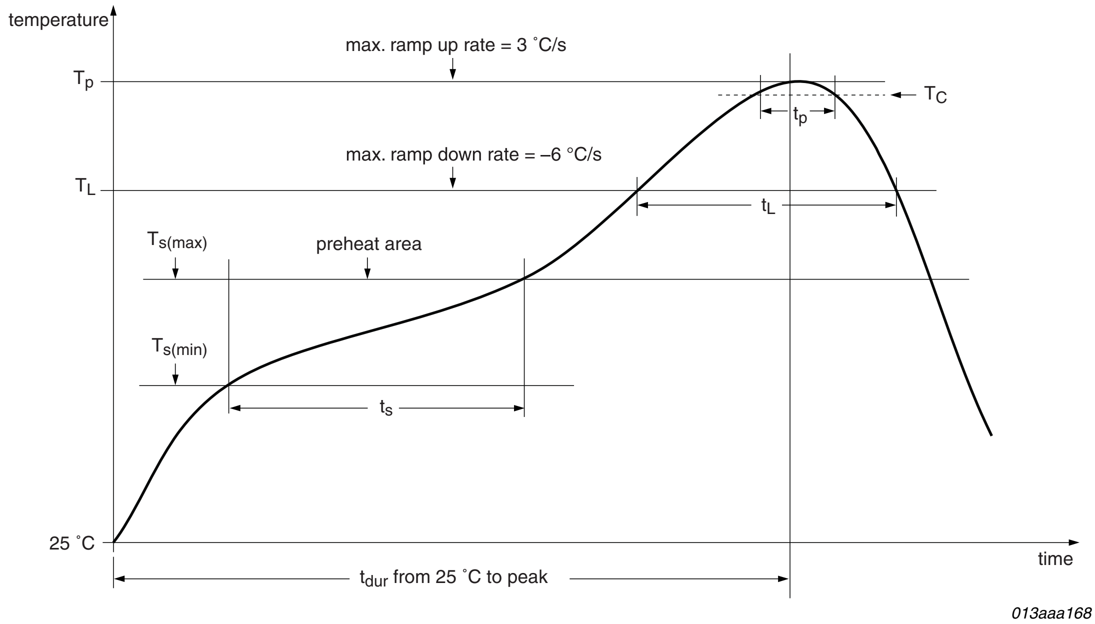


Figure not drawn to scale.

The appropriate values for this graph are shown in Table 6.

Remark: The reflow profile in this document is for classification/preconditioning and not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs, but must not exceed the parameters shown in Table 6.

Fig 3. Reflow temperature profile

Table 6. Values of reflow temperature profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during the reflow soldering process.

Symbol	Value	Unit
T_p	260	°C
T_L	217	°C
T_C	255	°C
$T_{s(max)}$	200	°C
$T_{s(min)}$	150	°C
t_p	30	s
t_L	60 to 150	s
t_s	60 to 120	s
t_{dur}	max 480	s

Recommendations:

1. The reflow soldering profile shown in Figure 3 is recommended. A full convection reflow system, capable of maintaining the reflow profile of Figure 3, is recommended.
2. The peak temperature (T_p) of the reflow soldering process must not exceed 260 °C. If the temperature exceeds 260 °C, the characteristics of the crystal oscillator will be degraded or even the device may be damaged.

3. The time, while the PCF212xA is heated above T_C = 255 °C, must not exceed 30 s (t_p), otherwise the characteristics of the crystal oscillator will be degraded or even the device may be damaged.

6.3 Effect of reflow soldering on the frequency characteristics

The reflow soldering process is typically generating a negative frequency shift.

After one-time reflow soldering, processed in accordance with the recommended temperature profile shown in Figure 3 and Table 6, a frequency shift of –5 ppm is typical. Any other reflow temperature profile or multiple soldering may cause a different frequency shift after soldering. The frequency shift after soldering can be reduced by lowering the peak temperature T_p and shortening the time t_p of the soldering process (see Figure 3 and Table 6).

6.4 Frequency correction after reflow soldering

In order to compensate for a shift in frequency due to reflow soldering, a frequency offset can be programmed through bits AO[3:0] of register address 19h (see Table 2 and Table 3). In the typical case and under consideration of the temperature profile as given in Figure 3, an offset of +5 ppm is considered to be most suitable. However, this may vary on a per case basis and in dependence of the actual soldering profile used.

Table 7. Frequency correction at 25 °C, typical

AO[3:0]		ppm
Decimal	**Binary**	
0	0000	+8
1	0001	+7
2	0010	+6
3	0011	+5
4	0100	+4
5	0101	+3
6	0110	+2
7	0111	+1
8	1000 [1]	0
9	1001	–1
10	1010	–2
11	1011	–3
12	1100	–4
13	1101	–5
14	1110	–6
15	1111	–7

[1] Default value.

Remark:

1. The typical frequency shift of –5 ppm, that occurs after a one-time reflow soldering processed in accordance with the recommended temperature profile shown in Figure 3 and Table 6, can be corrected by programming AO[3:0] = 0011.

2. A frequency measurement (see Section 5) should be performed after the final assembly of the board if
   - the soldering was processed multiple times,
   - the soldering was not made according to the recommended temperature profile,
   - the best result in accuracy should be achieved.

   Then the offset with the appropriate value given in Table 7 should be programmed into AO[3:0]. Deviations caused by assembly steps or due to production tolerances can be compensated with it.

7. Assembly recommendations

It is recommended to

- take precautions when using the PCF212xA with general-purpose mounting equipment in order to avoid excessive shocks that could damage the integrated quartz crystal
- avoid ultrasonic cleaning that could damage the integrated quartz crystal
- avoid in the board layout running signal traces under the package unless a ground plane is placed between the package and the signal line.

8. General application information

In general it can be said that

- the integration of the quartz crystal in the same package as the RTC has the following advantages:
  - elimination of crystal procurement issues
  - elimination of concerns regarding the crystal parameters matching those of the RTC
  - no more crystal PCB layout issues
- the IFS pin must be connected to ground (V_{SS}) to select the SPI-bus
- the IFS pin must be connected to the BBS pin to select the I^2C-bus
- a backup battery can be attached to the V_{BAT} pin to enable the battery switch-over when the main power V_{DD} fails. If V_{BAT} is not used, it has to be connected to ground
- the battery backed voltage V_{BBS} can be used to supply an external RAM to retain RAM data in battery backup mode. A low leakage decoupling capacitor should be connected from BBS to V_{SS}: suggested value is 1 nF, max 100 nF. If BBS is not used to supply an external IC the decoupling capacitor between the BBS and V_{SS} pins must always be connected
- CLKOUT and $\overline{\text{INT}}$ are open-drain, active LOW outputs which require external pull-up resistors: maximum pull-up voltage is 5.5 V
- the timestamp input pin $\overline{\text{TS}}$ can be connected to a push button for tamper detection (see Section 8.1).

8.1 Timestamp applications

The most common application of the timestamp function is tamper detection: date and time are stored when the cover of the equipment is opened. A push-button is attached to the cover in such a way, that when the cover is opened, the button is pushed (mechanical connection); the button is connected to the timestamp input pin so that when the button is pushed, the timestamp circuit detects the event, sets a flag and stores the date and time in internal registers.

The timestamp function integrated in the PCF212xA allows double tamper detection in an application, although with a single timestamp input pin: two push-buttons can be connected to the timestamp input pin. Time and date will be stored when one of the push-buttons will be pushed.

A typical application is an electrical meter, where one cover protects the terminal (terminal case) and another cover protects the electronics (electronic case) and an opening of each of them should be registered.

Figure 4 shows the double tamper detection application:

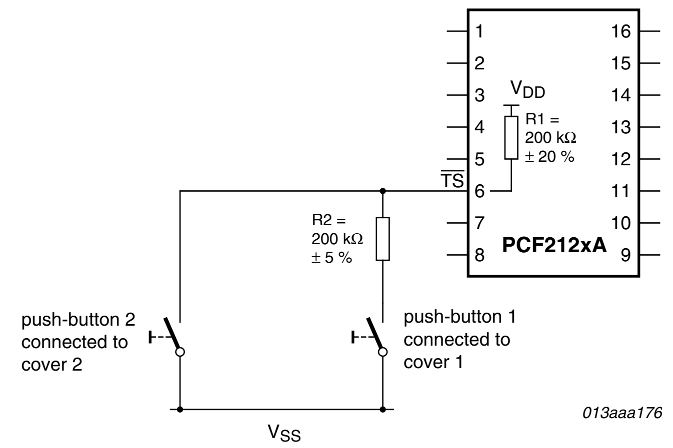


Fig 4. Tamper detection circuit with two push-buttons

- When cover 1 is opened, the push-button 1 is closed and the $\overline{TS}$ pin is driven to the intermediate level $V_{TS\_n} = \frac{R2}{R1 + R2} \times V_{DD} \cong \frac{V_{DD}}{2}$. For proper functionality R2 = 200 kΩ with a maximum variation of ±5 %.

  Event 1: TSF1 is set, date and time is registered.
- When cover 2 is opened, the push-button 2 is closed and the $\overline{TS}$ pin is driven to ground.

  Event 2: TSF1 and TSF2 are both set, date and time is registered.

8.2 Current consumption

Current consumption is reduced if the power management functions are disabled (PWRMNG[2:0] = 111). In that case the

- battery switch-over function is disabled
- battery low detection is disabled
- only one power supply (V_{DD}) is used.

9. Application information for PCF2127A

9.1 Timekeeping applications

PCF2127A used for the time keeping function (see Figure 5):

- No interface activity
- TS input floating or connected to BBS
- CLKOUT is disabled (COF[2:0] = 111)
- The power management functions are disabled (PWRMNG[2:0] = 111) and pin V_{BAT} is tied to ground
- The timestamp detection is disabled (TSOFF = 1)
- Interrupt (INT) and reset (RST) are connected to V_{DD} through pull-up resistors

Timekeeping is very accurate due to the temperature compensation. The power consumption is minimized.

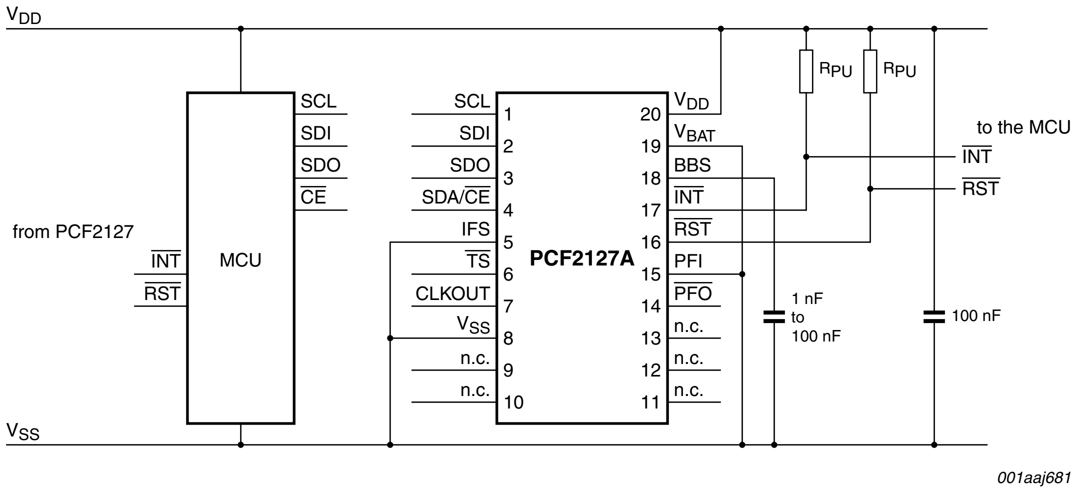


Fig 5. Application diagram: timekeeping

9.2 Timekeeping and CLKOUT

PCF2127A used for timekeeping and CLKOUT functions (see Figure 6):

- No interface activity
- $\overline{TS}$ input floating or connected to BBS
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32 kHz by default after start-up (COF[2:0] = 000)
- The power management functions are disabled (PWRMNG[2:0] = 111) and pin V_{BAT} is tied to ground
- The timestamp detection is disabled (TSOFF = 1)
- Interrupt ($\overline{INT}$) and reset ($\overline{RST}$) are connected to V_{DD} through pull-up resistors

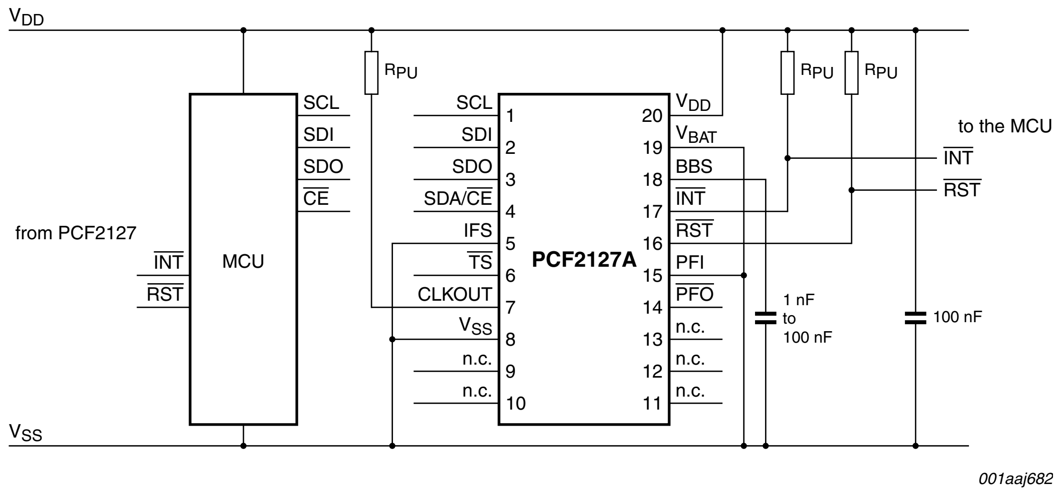


Fig 6. Application diagram: timekeeping and CLKOUT

9.3 Timekeeping, CLKOUT and power management

PCF2127A used for timekeeping and power management functions (see Figure 7):

- No interface activity
- $\overline{\text{TS}}$ input floating or connected to BBS
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin
- The battery switch-over, the battery low detection and the extra power fail detection functions are enabled by default (PWRMNG[2:0] = 000)
- The timestamp detection is disabled (TSOFF = 1)
- Interrupt ($\overline{\text{INT}}$), reset ($\overline{\text{RST}}$), and power fail output ($\overline{\text{PFO}}$) are connected to V_{DD} through pull-up resistors

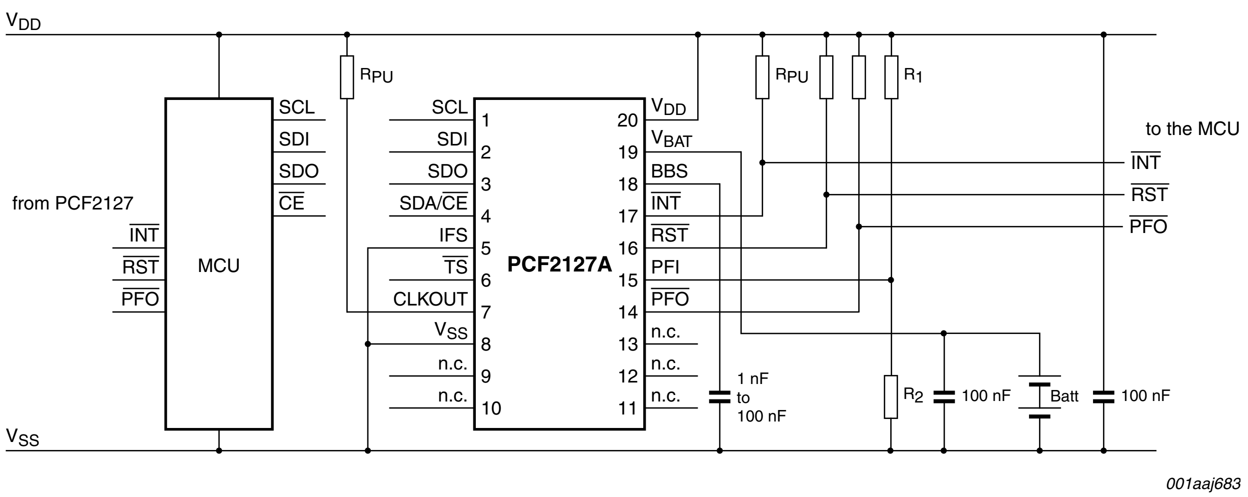


Fig 7. Application diagram: timekeeping, CLKOUT and power management

9.4 Timekeeping, CLKOUT, power management and timestamp

PCF2127A used for timekeeping, power management, CLKOUT and timestamp functions (see Figure 8):

- No interface activity
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin
- The battery switch-over, the battery low detection and the extra power fail detection functions are enabled by default (PWRMNG[2:0] = 000)
- The timestamp detection is enabled by default (TSOFF = 0)
- Interrupt ($\overline{INT}$), reset ($\overline{RST}$), and power fail output ($\overline{PFO}$) are connected to V_{DD} through pull-up resistors

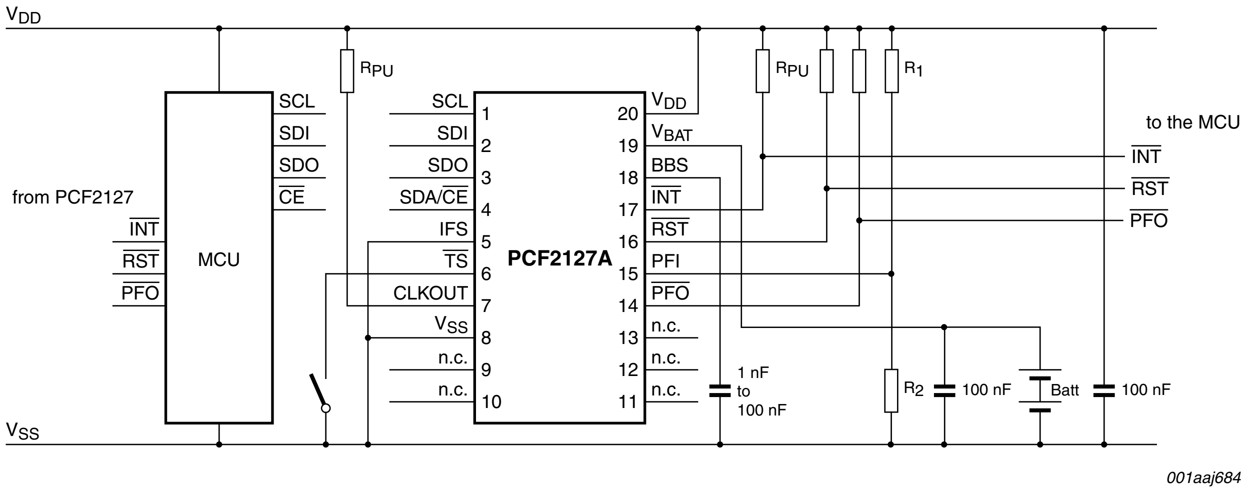


Fig 8. Application diagram: timekeeping, CLKOUT, power management and timestamp

9.5 Timekeeping, CLKOUT, timestamp and interface active

PCF2127A used for timekeeping, CLKOUT and timestamp functions (see Figure 9):

- Interface active
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32 kHz by default after start-up (COF[2:0] = 000)
- The power management functions are disabled (PWRMNG[2:0] = 111) and pin V_{BAT} is tied to ground
- The timestamp detection is enabled by default (TSOFF = 0)
- Interrupt ($\overline{INT}$) and reset ($\overline{RST}$) are connected to V_{DD} through pull-up resistors

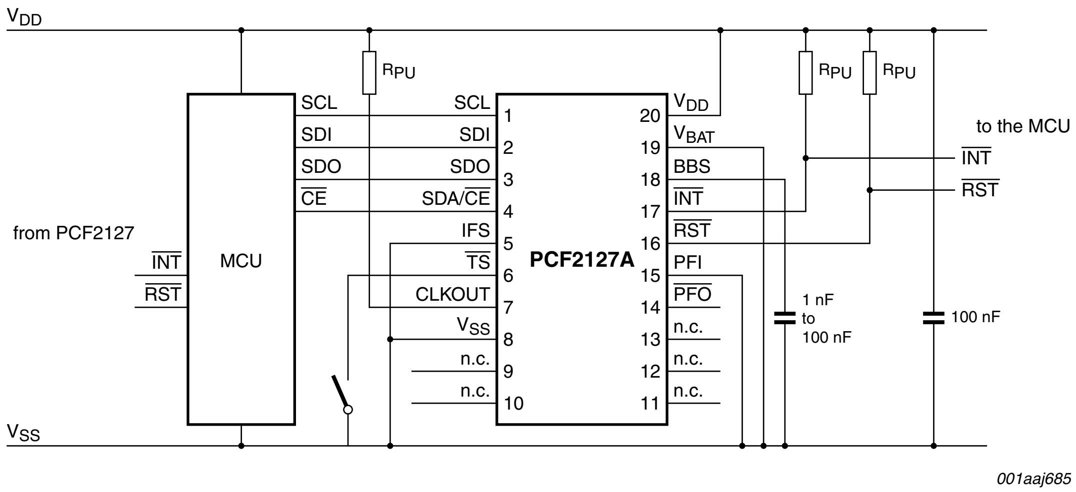


Fig 9. Application diagram: timekeeping, CLKOUT, timestamp with the interface active

9.6 Timekeeping, CLKOUT, power management, timestamp and interface active

PCF2127A used for timekeeping, power management, CLKOUT and timestamp functions (see Figure 10):

- Interface active
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin
- The battery switch-over, the battery low detection and the extra power fail detection functions are enabled by default (PWRMNG[2:0] = 000)
- The timestamp detection is enabled by default (TSOFF = 0)
- Interrupt ($\overline{INT}$) and reset ($\overline{RST}$) and the power fail output ($\overline{PFO}$) are connected to V_{DD} through pull-up resistors
- BBS supplies an external device, e.g. SRAM (see Figure 10) or a microcontroller (see Figure 11)

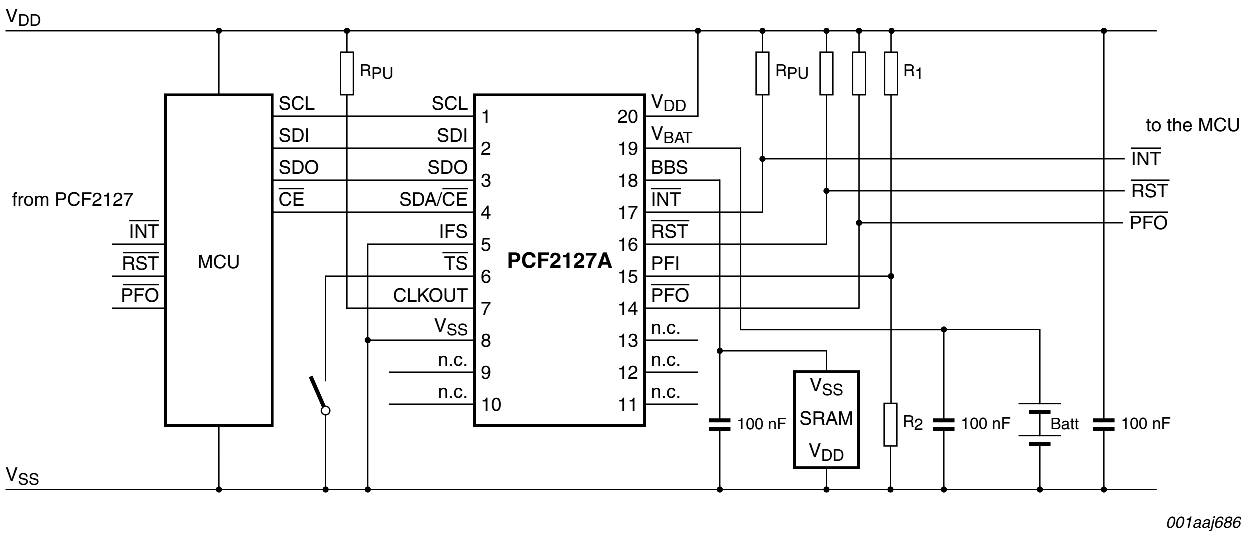


Fig 10. Application diagram: timekeeping, CLKOUT, power management, timestamp with the interface active

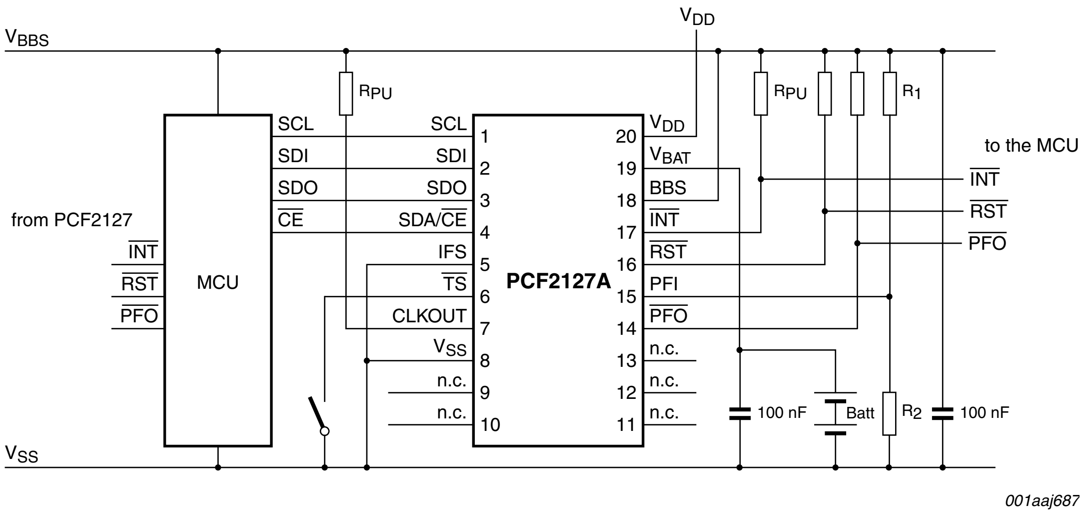


Fig 11. Application diagram: BBS supplies the microcontroller

10. Application information for PCF2129A

10.1 Timekeeping applications

PCF2129A used for the time keeping function (see Figure 12):

- No interface activity
- CLKOUT is disabled (COF[2:0] = 111)
- The power management functions are disabled (PWRMNG[2:0] = 111) and pin V_{BAT} is tied to ground
- The timestamp detection is disabled (TSOFF = 1)

Timekeeping is very accurate due to the temperature compensation. The power consumption is minimized.

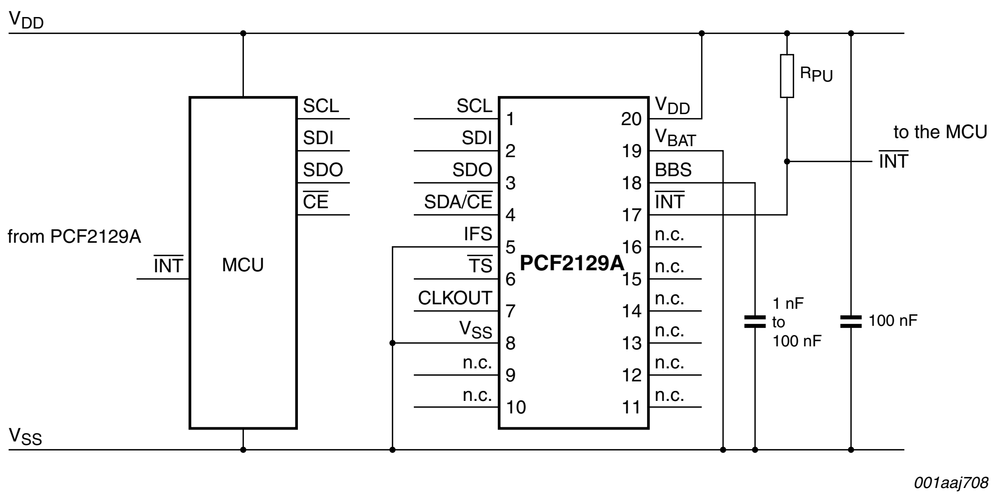


Fig 12. Application diagram: timekeeping

10.2 Timekeeping and CLKOUT

PCF2129A used for timekeeping and CLKOUT functions (see Figure 13):

- No interface activity
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- The power management functions are disabled (PWRMNG[2:0] = 111) and pin V_{BAT} is tied to ground
- The timestamp detection is disabled (TSOFF = 1)

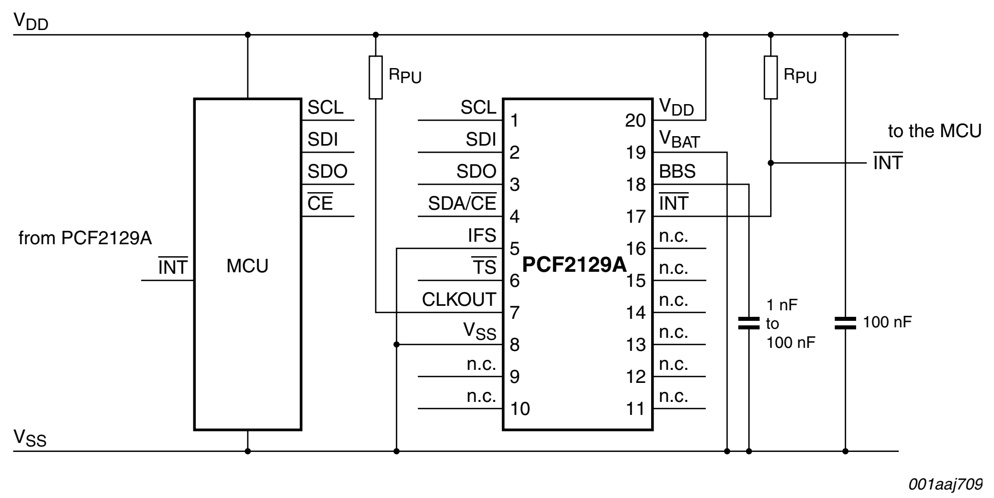


Fig 13. Application diagram: timekeeping and CLKOUT

10.3 Timekeeping, CLKOUT and power management

PCF2129A used for timekeeping and power management functions (see Figure 14):

- No interface activity
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin
- The battery switch-over and the battery low detection functions are enabled by default (PWRMNG[2:0] = 000)
- The timestamp detection is disabled (TSOFF = 1)

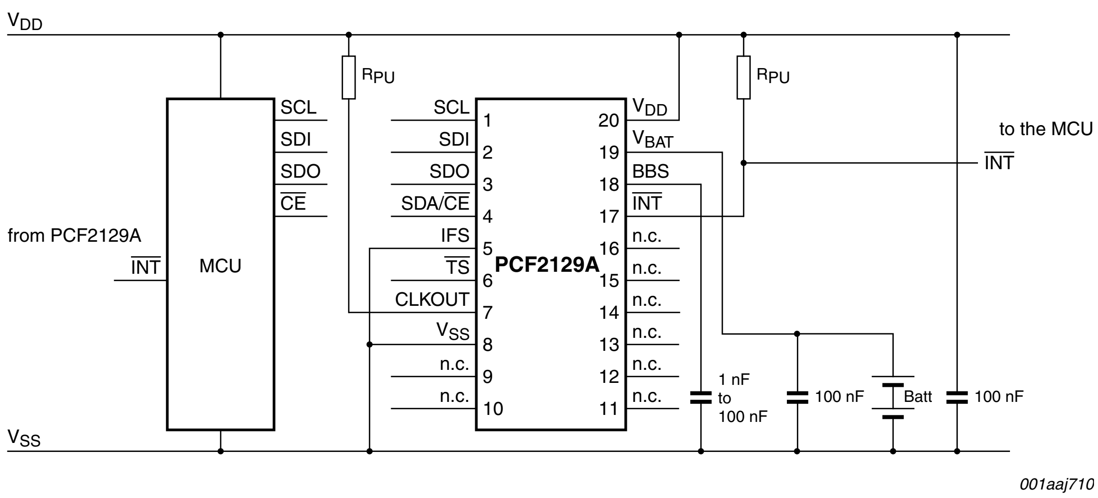


Fig 14. Application diagram: timekeeping, CLKOUT and power management

10.4 Timekeeping, CLKOUT, power management and timestamp

PCF2129A used for timekeeping, power management, CLKOUT and timestamp functions (see Figure 15):

- No interface activity
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin
- The battery switch-over and the battery low detection functions are enabled by default (PWRMNG[2:0] = 000)
- The timestamp detection is enabled by default (TSOFF = 0)

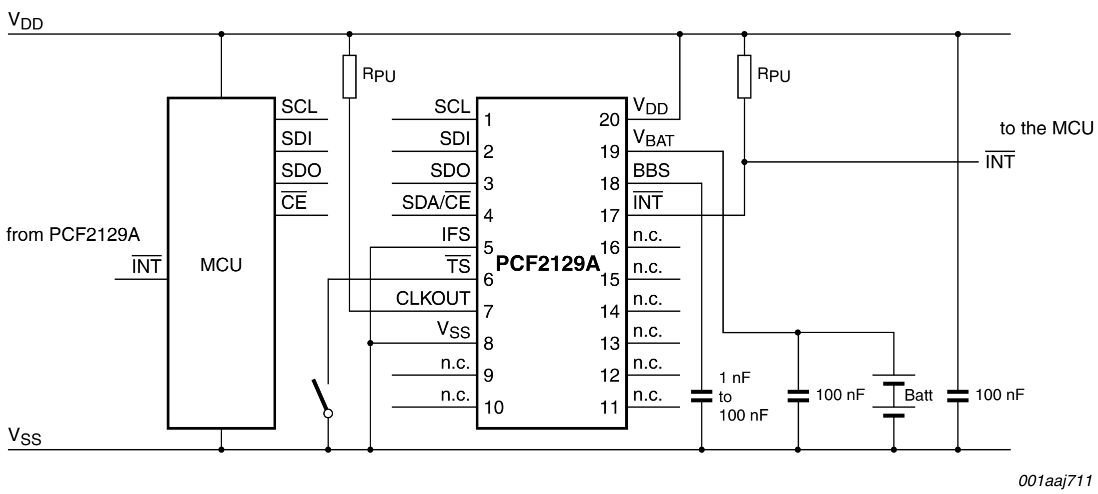


Fig 15. Application diagram: timekeeping, CLKOUT, power management and timestamp

10.5 Timekeeping, CLKOUT, timestamp and interface active

PCF2129A used for timekeeping, CLKOUT and timestamp functions (see Figure 16):

- Interface active
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- The power management functions are disabled (PWRMNG[2:0] = 111) and pin V_{BAT} is tied to ground
- The timestamp detection is enabled by default (TSOFF = 0)

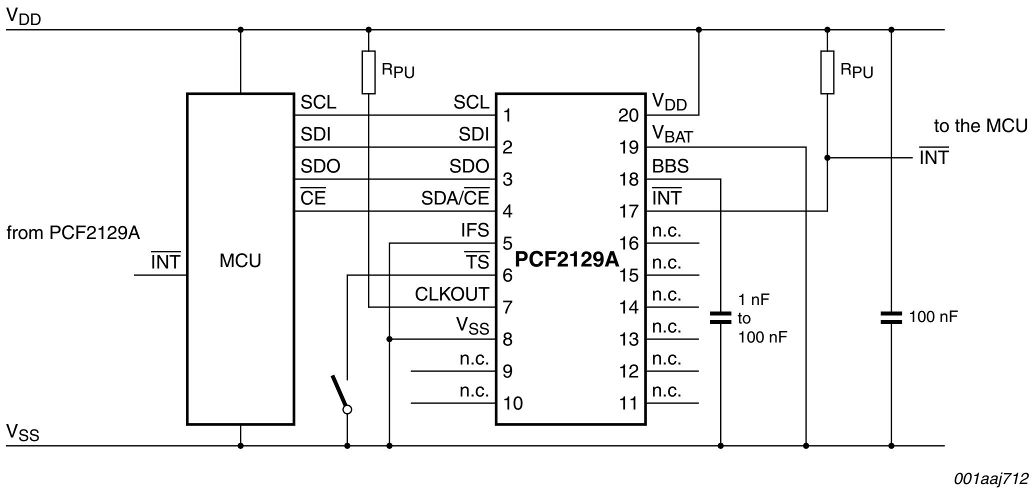


Fig 16. Application diagram: timekeeping, CLKOUT, timestamp with the interface active

10.6 Timekeeping, CLKOUT, power management, timestamp and interface active

PCF2129A used for timekeeping, power management, CLKOUT and timestamp functions (see Figure 17):

- Interface active
- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin
- The battery switch-over and the battery low detection functions are enabled by default (PWRMNG[2:0] = 000)
- The timestamp detection is enabled by default (TSOFF = 0)
- BBS supplies an external device, e.g. SRAM (see Figure 17) or a microcontroller (see Figure 18)

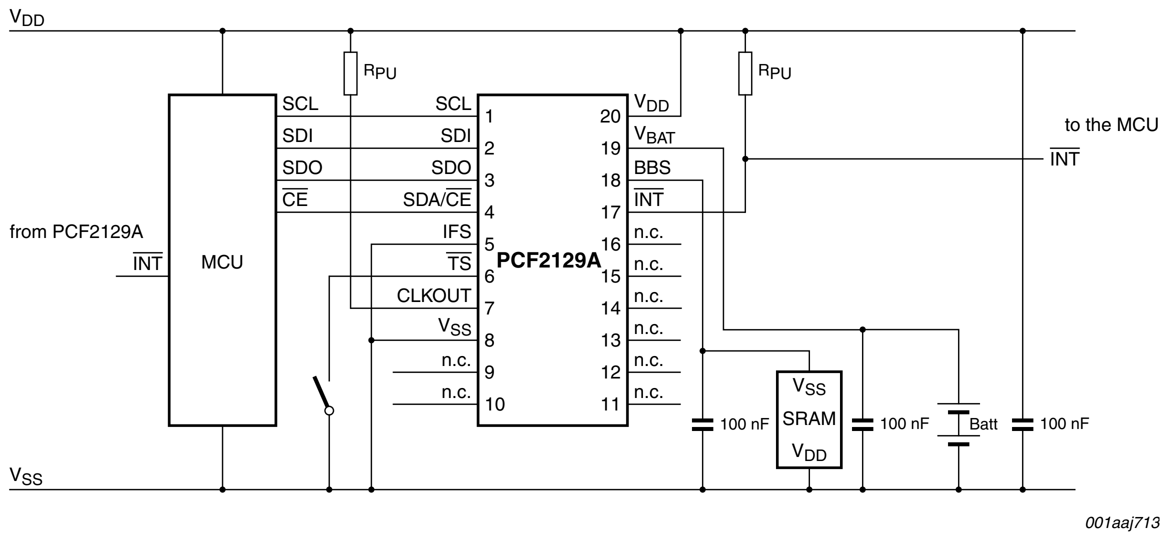


Fig 17. Application diagram: timekeeping, CLKOUT, power management, timestamp with the interface active

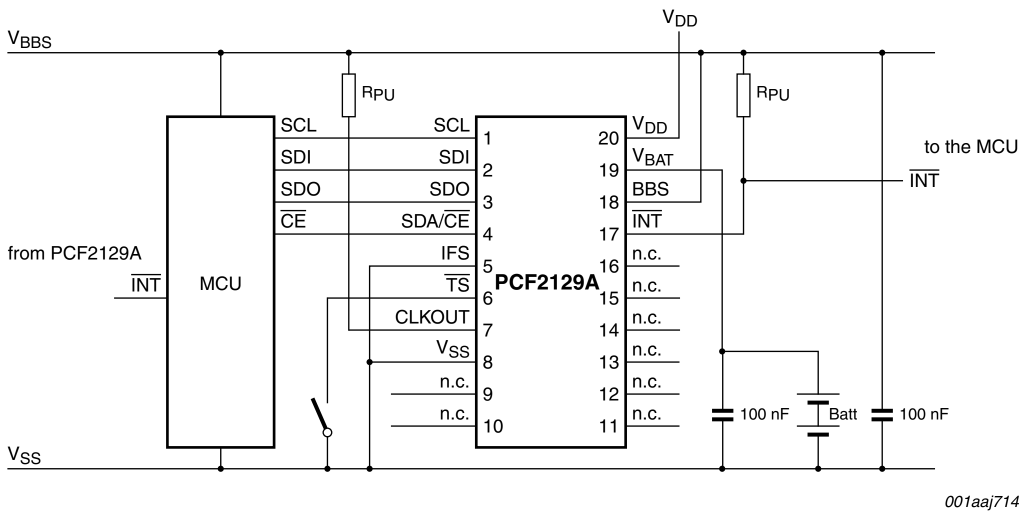


Fig 18. Application diagram: BBS supplies the microcontroller

11. Abbreviations

Table 8. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
MCU	Microcontroller Unit
PCB	Printed-Circuit Board
PPM	Parts Per Million
RAM	Random Access Memory
RTC	Real Time Clock
SMD	Surface Mount Device
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TCXO	Temperature Compensated Xtal Oscillator
Xtal	crystal

12. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[3] **IPC/JEDEC J-STD-020 —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[4] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[5] **PCF2127A —** Integrated RTC, TCXO and quartz crystal, Data Sheet

[6] **PCF2129A —** Integrated RTC, TCXO and quartz crystal, Data Sheet

[7] **SNW-SQ-623 —** NXP store and transport conditions

[8] **UM10204 —** I^2C-bus specification and user manual

[9] **UM10301 —** User Manual for NXP Real Time Clocks PCF85x3, PCA8565 and PCF2123, PCA2125

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14. Contents

Date of release: 11 December 2009
Document identifier: AN10857_1